REMARKS/ARGUMENTS

Claim 20 was rejected under 35 USC §112 as failing to comply with the enablement requirement. This rejection is respectfully traversed. The applicants observe that "signal of type ECL" corresponds to a well defined and known standard for digital signals, compatible with a known family of digital circuits. This standard, tailored for high-speed applications, foresees a "0" level of -0.9V and a "1" level of -1.75V and is around since about 1968. It is submitted that the skilled person would have no difficulty to make a clock generating circuit compatible with ECL signals. Please find enclosed a copy of a passage from "The Art of Electronics," by Horowitz and Hill, published on 1989, with a reference to the ECL standard.

Claims 1, 3-15, 19, 22-30 were rejected under 35 USC 103(a) as being unpatentable over Olarig et al in view of Salo et al. This rejection is respectfully traversed. Olarig deals with a computer bus capable of "hot-plugging" memory modules, that is to say a data bus in which memory modules can be inserted without turning the system off. This reference describes a purely digital device, not dealing with analog signals. Ths applicants, on the other hand, propose a high-speed digitizer. This is a special device which deals with both high-speed logic and analog signals. These devices are peculiar in that they require extremely high speed and low amplitude noise at the same time.

Since no analog signals are involved, the device described by Olarig does not have an analog input and, as the examiner acknowledges, does not include analog/digital converters. On the contrary, the present invention comprises an analog input, and an analog/digital converter for digitizing an analog signal therefrom.

In Olarig the connection between the bus and each memory module takes place at one single memory slot connector, and in a corresponding connector on one side of the memory module. According to column 6, lines 36-48 of this reference, the memory slot connector includes power, clock and bus lines. The data

acquisition modules of the present invention, instead, have a separate connector, placed on another side of the module (in practice on the front side), for connecting to a synchronization bus.

Salo describes a digital wireless modem implemented in an expansion card (a PCMCIA card) comprising two transmission buses, one for control and data signal, the other for digital audio signal. This reference deals with digital audio signal and does not disclose an analog input, in contrast with the present invention. Also this reference does not include a synchronization bus, much less a separate connector for a synchronization bus, like the present invention. This reference however cites analog-digital converters for converting audio signal into digital signals.

With respect to the alleged obviousness over Olarig in view of Salo, neither the references themselves nor some other prior art suggest that they be combined. The mere mention that ADC may be used to convert an analog signal made by Salo can not constitute an incitation to combine these two references.

Additionally, the applicants observe that Olarig and Salo belong to a different field than the applicant's invention. It is not realistic to assume that a skilled person would know and consult all the documents pertaining to electronics in order to improve a data acquisition module. Considering the evolution of modern electronics the fields of mixed analog-digital techniques and fast analog signal treatment must be considered as distinct from those of computer or wireless modems. Olarig and Salo belong to two distinctly nonanalogous fields to that of the present invention.

Moreover, even if one were to combine the teaching of Olarig and Salo, the resulting combination would be inoperative, since there are no analog signals, in the device of Olarig, which could be digitalized by the analog-digital converter allegedly suggested by Salo.

Furthermore, even if one could succeed in obtaining an operative combination of the two references above, the results would still not meet the claims,

since it would lack the claimed analog input and the claimed separate connector for a synchronization bus.

With respect to the further application of Shah to claim 2, Shah describes another but controller for "hot plugging" much like the one treated by Olarig. This system as well does not contain an analog input, or an analog-digital converter, or a separate connector for a synchronization bus placed on another side of the module.

Since claim 1 is now in condition for allowance, it is submitted that the remaining claims, all dependent on claim 1, are also patentable.

If there are any fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. 33307.

Respectfully submitted,
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